Remarks

The applicant does not propose any amendment of claims 2, 3, 5 to 12 & 14 to 17 as currently pending in the application. It is the applicant's view that the claims as currently pending patentably distinguish the present invention over the prior art of record as will become apparent from the following submission.

The present invention concerns a functional partitioning of an ATM adaptation layer to enable different traffic services to be carried over different adaptation layers, for example AAL1, AAL2 & AAL5, and to support AAL2 switching. A key requirement of any adaptation layer partitioning is that it optimizes buffering apportionment in order to minimize delays and to minimize the amount of memory resources employed and hence the cost of implementation (refer page 2, lines 20 to 32).

The present invention addresses this object by providing a **common part sublayer (CPS) ATM adaptation device** incorporating ingress and egress paths respectively to and from a broadband (ATM) network. Buffer storage (memory) is required in the CPS ATM adaptation device ingress path for reasons of scheduling ATM cells to the ATM network according to traffic class and priority and to control the assembly of AAL2 mini-packets into ATM CPS payload data units (PDUs) (refer page 8, lines 23 to 32). As such, the CPS ingress path has a **common** memory (primary buffer) for payload storage incorporated therein. In a preferred embodiment of the invention, an optional memory is incorporated into a service specific convergence sublayer (SSCS) (part of the) ingress path for reasons of storing fragmented SDUs etc although the present invention as defined by independent claims 2, 12, 16 & 17 is not limited by this feature.

In contrast to the CPS ingress path, the CPS egress path operates as a through-flow path, i.e. does not incorporate memory for payload storage purposes.

In the preferred embodiment of the invention, a primary buffer is incorporated into a SSCS egress path but once again the present invention as defined by the currently pending independent claims is not limited by this feature.

One advantage of having the CPS egress path operate as a flow-through path is that, for AAL2 switching applications, traffic received on the CPS egress path can be immediately re-routed to the CPS ingress path without being unnecessarily delayed by buffering on the CPS egress path. Such traffic will be buffered in the common memory of the CPS ingress path prior to being re-transmitted on the broadband network. In the preferred embodiment of the invention incorporating a primary buffer in the SSCS egress path, traffic flowing through the CPS egress path which is not switched to the CPS ingress path is buffered prior to being disassembled.

The Examiner has maintained his rejection of the currently pending claims under 35 U.S.C. 103(a) as being unpatentable over Westberg et al (US 5,946,309) in view of Westberg (US 6,195,353).

The Examiner's position can be neatly summarized as "*Only the teachings relating to the scheduling and prioritization that involve the input buffer taught by Westberg are being incorporated into the system of Westberg et al*" (final office action, page 6, final part of "Response to arguments"). The presumption underlying this position is that Westberg et al teaches all other features of the present invention as defined by the currently pending independent claims. This is not so.

To establish a prima facie case of obviousness, it is necessary to show that the prior art references teach or suggest all of the claim limitations. Westberg at al does not teach the functional partitioning of a common part sublayer ATM adaptation device. While this prior art reference teaches a system that utilizes the ATM adaptation layer, it neither suggests nor even mentions the possibility that

buffer apportionment can be addressed with respect to the common part sublayer (CPS) ingress and egress paths of the ATM adaptation layer. The same can be said for Westberg. On this basis alone, the rejection under 35 U.S.C. 103(a) cannot be sustained.

Also, the Examiner contends that, since Westberg et al does not mention buffering the incoming data to the receiving station, it can be considered as a "through path". The applicant again contests this conclusion on the grounds that the complete absence in a prior art reference of any discussion of a feature as claimed in the invention cannot be said to have satisfied the test that the prior art reference teaches or suggests the feature. At best, the reference is ambiguous with respect to this feature but the applicant maintains as entirely pertinent those parts of its previous response that addresses this issue and considers that these have not been properly addressed.

Issue is also taken with the Examiner's conclusion as to what Westberg teaches. It is apparent from Westberg, col. 3, line 61 to col. 4, line 60 that there is provided an input buffer 530 for each circuit emulation connection 525 wherein the function of the input buffer 530 is to allow the operator, in association with a packetization clock period, to control the length of the short packets extracted from the input buffer 530 for that circuit 525 (col. 4, lines 17 to 20). Short packets from the input buffer 530 can then be multiplexed with short packets extracted from the input buffers 530 of other circuits 525. Consequently, Westberg does not teach the provision of a ***common*** *memory for* payload storage in the CPS ingress path in order to perform multiplexing at both the AAL and ATM layers. Therefore the rejection under 35 U.S.C. §103(a) cannot be sustained.

It is respectfully submitted therefore that for foregoing reasons the present invention is not obvious having regard to a combination of the Westberg citations.

Favorable reconsideration of the currently pending claims is hereby requested.

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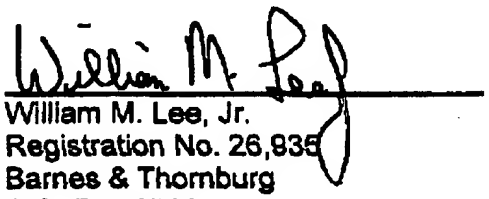
Respectfully submitted,



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